REMARKS

Claims 1-9 are pending in this application.

Rejection of claims 1-9 under 35 U.S.C. 103(a)

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) (European Patent Application No. EP-1128673) in view of Dean et al. (U.S. Patent No. 5,914,757), hereinafter "Dean."

The present claimed arrangement provides a video apparatus. A digital encoder receives a first analog signal with ancillary information in a given time window and generates on an output, a digital stream based at least partly on the first analog signal. A digital decoder is at least connectable to the output and generates a second analog signal from the digital stream at least when connected to the output. A control device determines the occurrence of the time window and generates a corresponding control signal. Based on the control signal, the first analog signal is selectively output when the time window occurs. Otherwise, the second analog signal is selectively output. The digital decoder includes means for synchronizing the second analog signal to the first analog signal. AAPA and Dean, when taken individually or in combination, do not disclose or suggest the features of claim 1 of the present arrangement.

AAPA describes a video apparatus having a first, second and third circuit. The first circuit generates a first baseband analog video signal on a first output. The second circuit is connectable to the first output and can digitise the first baseband analog video signal and process and output a corresponding digital stream on a second output. The second output is connectable to the third circuit generating on a third output a second baseband analog video signal on the basis of the digital stream (*see* Abstract).

AAPA neither discloses nor suggests "a digital encoder receiving a first analogue signal with **ancillary** information in **a given time window**" as recited in claim 1 of the present arrangement. AAPA describes "[a] digital encoder 116 [that] receives the analog signal from the analog source 112 and outputs a digital stream" (paragraph [0022]). However, nowhere in AAPA is there suggestion or disclosure of "a digital encoder receiving a first analogue signal

with ancillary information in a given time window" as recited in claim 1 of the present arrangement. AAPA describes an analog and digital source. "The analog source 112 could also be for instance the output of a conventional analog VCR" (paragraph [0020]). "The digital source 114 can be a digital tuner receiving from an antenna or a cable-link a video signal which is digitally coded for transmission, for instance according to the MPEG-II format" (paragraph [0021]). However, AAPA nowhere discloses or suggests that "a first analogue signal" is received "with ancillary information" and "in a given time window" as recited in claim 1 of the present arrangement. Additionally, AAPA neither discloses nor suggests "control means for determining the occurrence of said time window and correspondingly generating a control signal ... selecting means for selectively outputting, based on said control signal, the first analogue signal, when said time window occurs, and otherwise, the second analogue signal, wherein the digital decoder includes means for synchronising the second analogue signal to the first analogue signal" as recited in claim 1 of the present arrangement. The Office Action on page 2 correctly admits that "AAPA does not explicitly recite synchronizing the second analog to the first analog signal, nor the determining the occurrence of said time window." However, Applicants respectfully submit that combining AAPA with the system of Dean, as suggested by the Office Action, would not make the present claimed arrangement unpatentable.

Dean describes a slow Phase Locked Loop (PLL) that is utilized to prevent an abrupt change to a video display containing multiple images, when the source of the synchronization is changed. Such displays include Picture in Picture (PIP) television systems and computer displays. By appropriate buffering and memory management, visual disruptions can be minimized by slowly synchronizing the display synchronization signals to the new synchronization source. The slow synchronization also produces a less disruptive visual image when the source, or channel, of a single image display is changed, and allows for smooth visual transitions on displays having inertial elements, such as color wheels (*see* Abstract).

Dean (with AAPA) neither discloses nor suggests "control means for determining the occurrence of said time window and correspondingly generating a control signal ... selecting means for selectively outputting, based on said control signal, the first analogue signal, when said time window occurs, and otherwise, the second analogue signal" as recited in claim 1 of the

present arrangement. Neither Dean nor AAPA, when taken individually or in combination, disclose or suggest "a digital encoder receiving a first analogue signal with ancillary information in a given time window" as recited in claim 1 of the present arrangement. Therefore, Dean and AAPA cannot disclose or suggest "control means for determining the occurrence of said **time window** and correspondingly generating a control signal" as recited in claim 1 of the present arrangement. Additionally, although Dean, in Fig. 2 cited by the Office Action, shows synchronizing of two analog video signals, Fig. 2 does not disclose or suggest "a first analogue signal with ancillary information in a given time window and generating on an output a digital stream based at least partly on the first analogue signal" as recited in claim 1 of the present arrangement. In addition, Fig. 4 of Dean shows "[a] multiple input system ... The input channels, 461 through 464, may each have a different format" (col. 10, lines 20-22). However, in Fig. 4, analog signals (i.e. 463 and 464) are converted to digital via the "A/D" converter block. After the conversion, the digital signals are synchronized. This is wholly unlike the present claimed arrangement in which "the digital decoder includes means for synchronising the second analogue signal to the first analogue signal."

Furthermore, Dean, similar to AAPA, does not disclose or suggest "selecting means for selectively outputting, based on said control signal, the first analogue signal, when said time window occurs, and otherwise, the second analogue signal" as recited in claim 1 of the present arrangement. Dean describes outputting a synchronization signal 102 to the video display 100. Additionally, the output of mixer 150 is connected to the video display 100. However, Dean does not disclose or suggest "selecting means for selectively outputting, based on said control signal, the first analogue signal, when said time window occurs, and otherwise, the second analogue signal" as recited in claim 1 of the present arrangement. A selection between a first and second analog signal, based on a time window occurrence, is neither disclosed nor suggested by Dean. Therefore, Dean (with AAPA) does not disclose or suggest the features of claim 1 of the present arrangement.

Even if a combination of the systems of AAPA and Dean could be made, as suggested by the Office Action, the combination would not make the present claimed arrangement unpatentable. The combination of AAPA and Dean would yield a system containing a digital

decoder that would receive an analog signal and output a digital signal. A second analog signal may also be converted to a digital signal through an A/D converter. The two signals may be synchronized with one another. However, synchronization would occur after the signals are converted to digital. The combined system would not disclose or suggest "a digital encoder receiving a first analogue signal with ancillary information in a given time window and generating on an output a digital stream based at least partly on the first analogue signal" as recited in claim 1 of the present arrangement. Because the combined system is not concerned with a given time window, the combined system would also not disclose or suggest "control means for determining the occurrence of said time window and correspondingly generating a control signal" as recited in claim 1 of the present arrangement. Additionally, the combined system would not disclose or suggest "selecting means for selectively outputting, based on said control signal, the first analogue signal, when said time window occurs, and otherwise, the second analogue signal." Moreover, although the combined system may describe a digital decoder, the digital decoder would be unable to synchronize "the second analogue signal to the first analogue signal" as the combined system only synchronizes two digital signals after the signals are converted from analog to digital. Therefore, the combined system of AAPA and Dean would not make the present claimed arrangement unpatentable. Consequently, withdrawal of the rejection of claim 1 under 35 U.S.C. 103(a) is respectfully requested.

Claim 2 is dependent on claim 1 is and is considered patentable for the same reasons presented above with respect to claim 1. Claim 2 is also considered patentable because Dean and AAPA neither disclose nor suggest that "the means for synchronising the second analogue signal to the first analogue signal are coupled to a synchronisation separator receiving the first analogue signal on an input" as recited in claim 2 of the present arrangement. As described above with respect to claim 1, the synchronization of signals described in Dean is only performed for digital signals. Additionally, nowhere in Dean and AAPA is there any suggestion or disclosure of the "means for synchronising the second analogue signal to the first analogue signal ... [being] coupled to a **synchronisation separator** receiving the first analogue signal on an input" as recited in claim 2 of the present arrangement. As seen in Fig. 4 of Dean, "sync control block 420 ... select[s] one of the synchronization signals 371 through 374 for synchronizing the display and memory elements" (col. 10, lines 28-30). The synchronization of the digital signals in Dean

(with AAPA) do not disclose or suggest that "means for synchronising the second analogue signal to the first analogue signal are coupled to a synchronisation separator receiving the first analogue signal on an input" as recited in claim 2 of the present arrangement. Consequently, withdrawal of the rejection of claim 2 under 35 U.S.C. 103(a) is respectfully requested.

Claims 3-8 are dependent on claim 1 and are considered patentable for the reasons presented above with respect to claim 1. Consequently, withdrawal of the rejection of claims 3-8 under 35 U.S.C. 103(a) is respectfully requested.

Independent claim 9 provides a video apparatus including a digital encoder and a digital decoder. The digital decoder receives a first analog signal and generates on an output, a digital stream based on the first analog signal. The digital decoder receives the digital stream and generates a second analog video signal based on the digital stream and synchronized with the first analog signal. The digital decoder synchronizes the second analog signal to the first analog signal. AAPA and Dean, when taken individually or in combination, do not disclose or suggest the features of claim 9 of the present arrangement.

AAPA describes a video apparatus having a first, second and third circuit. The first circuit generates a first baseband analog video signal on a first output. The second circuit is connectable to the first output and can digitise the first baseband analog video signal and process and output a corresponding digital stream on a second output. The second output is connectable to the third circuit generating on a third output a second baseband analog video signal on the basis of the digital stream (*see* Abstract).

AAPA neither discloses nor suggests "a digital decoder receiving the digital stream and generating a second analogue video signal based on the digital stream and synchronised with the first analogue signal, wherein the digital decoder includes means for synchronising the second analogue signal to the first analogue signal" as recited in claim 9 of the present arrangement. AAPA describes "[a] digital encoder 116 [that] receives the analog signal from the analog source 112 and outputs a digital stream" (paragraph [0022]). AAPA also describes an analog and digital source. "The analog source 112 could also be for instance the output of a conventional analog

VCR" (paragraph [0020]). "The digital source 114 can be a digital tuner receiving from an antenna or a cable-link a video signal which is digitally coded for transmission, for instance according to the MPEG-II format" (paragraph [0021]). However, nowhere in AAPA is there suggestion or disclosure of "a digital decoder receiving the digital stream and generating a second analogue video signal based on the digital stream and synchronised with the first analogue signal, wherein the digital decoder includes means for synchronising the second analogue signal to the first analogue signal" as recited in claim 9 of the present arrangement. The Office Action on page 3 correctly admits that "AAPA does not explicitly recite synchronizing the second analog to the first analog signal." However, Applicants respectfully submit that combining AAPA with the system of Dean, as suggested by the Office Action, would not make the present claimed arrangement unpatentable.

Dean describes a slow Phase Locked Loop (PLL) that is utilized to prevent an abrupt change to a video display containing multiple images, when the source of the synchronization is changed. Such displays include Picture in Picture (PIP) television systems and computer displays. By appropriate buffering and memory management, visual disruptions can be minimized by slowly synchronizing the display synchronization signals to the new synchronization source. The slow synchronization also produces a less disruptive visual image when the source, or channel, of a single image display is changed, and allows for smooth visual transitions on displays having inertial elements, such as color wheels (*see* Abstract).

Dean (with AAPA) neither discloses nor suggests "a digital decoder receiving the digital stream and generating a second analogue video signal based on the digital stream and synchronised with the first analogue signal" as recited in claim 9 of the present arrangement. Dean, in Fig. 2 cited in the Office Action, shows synchronizing of two analog video signals. However, Fig. 2 of Dean does not disclose or suggest "a digital encoder receiving a first analogue signal and generating on an output a digital stream based on the first analogue signal" as recited in claim 9 of the present arrangement. In addition, Fig. 4 of Dean shows "[a] multiple input system ... The input channels, 461 through 464, may each have a different format" (col. 10, lines 20-22). However, in Fig. 4, analog signals (i.e. 463 and 464) are converted to digital via the "A/D" converter block. After the conversion, the digital signals are synchronized. This

is wholly unlike the present claimed arrangement in which "a digital decoder receiving the digital stream and generating a second analogue video signal based on the digital stream and synchronised with the first analogue signal, wherein the digital decoder includes means for synchronising the second analogue signal to the first analogue signal." Therefore, Dean (with AAPA) does not disclose or suggest the features of claim 9 of the present arrangement.

Even if a combination of the systems of AAPA and Dean could be made, as suggested by the Office Action, the combination would not make the present claimed arrangement unpatentable. The combination of AAPA and Dean would yield a system containing a digital decoder that would receive an analog signal and output a digital signal. A second analog signal may also be converted to a digital signal through an A/D converter. The two signals may be synchronized with one another, however, synchronization would occur after the signals are converted to digital. The digital decoder in the combined system would not disclose or suggest "receiving the digital stream and generating a second analogue video signal based on the digital stream and synchronised with the first analogue signal" and would be unable to synchronize "the second analogue signal to the first analogue signal" as the combined system only synchronizes two digital signals after the signals are converted from analog to digital. Therefore, the combined system of AAPA and Dean would not make the present claimed arrangement unpatentable. Consequently, withdrawal of the rejection of claim 9 under 35 U.S.C. 103(a) is respectfully requested.

In view of the above remarks, it is respectfully submitted that this rejection is satisfied and should be withdrawn.

Having fully addressed the Examiner's rejections, it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at the phone number below, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No other fee is believed due. However, if an additional fee is due, please charge the fee to Deposit Account 07-0832.

Respectfully submitted,
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